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EXAMINER	
GU, SHAWN X	

ART UNIT	PAPER NUMBER
2189	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/769,586	LOWE, ERIC E.	
	Examiner	Art Unit	
	Shawn Gu	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☒ Claim(s) *28 and 29* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 March 2004 and 30 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

1. The oath or declaration is defective. A new oath or declaration in compliance with 37 CFR 1.67(a) identifying this application by application number and filing date is required. See MPEP §§ 602.01 and 602.02.

The oath or declaration is defective because: the claim for priority benefit under 35 U.S.C 119(e) did not include the application number of the provisional application, the attorney docket number is listed instead. The claimed priority benefit does not interfere with the references cited in this Office Action.

Specification

2. The specification is objected to for the following informalities:

On page 1, line 9, the U.S. Application Serial Number is missing.

Appropriate correction is required.

Claim Objections

3. Claims 2, 3, 8-10, 13-21 and 26-29 are objected to because of the following informalities:

As for claims 2 and 3, "D) (1)" on line 1 of claim 2 should be changed to "D) (i)".

As for claims 8-10, the acronym "TTE" should be spelled out as "translation table entry" as it is mentioned for the first time in the claim.

As for claims 13-21, the acronym "CPU" should be spelled out as "central processing unit" as it is mentioned for the first time in the claim.

As for claims 26-29, the phrase "the-miss" should be "the miss", and the phrase "a TSB resizing event" should be changed to "and a TSB resizing event". In addition, the acronym "TSB" should be spelled out as "translation storage buffer" as it is mentioned for the first time in the claim.

All dependent claims are rejected as having the same deficiencies as the claims they depend from.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 8-10 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

As for claims 8-10, according to the specification, TLB Miss Handler is a piece of software yet it is only invoked after a search and a miss in the TLB (see Page 11, Lines 19-23), and the invention can be embodied as computer readable code (see Page 21, Lines 27-30). However, the invention is a method of handling a TLB miss, which takes place after searching the TLB. It is disclosed by the specification that TLB is searched when a memory access instruction is initiated (see Page 12, lines 25-30), but it does not disclose computer program code instructions are used for searching a TLB for a TLB entry. According to the specification, the TLB is merely searched.

All dependent claims are rejected as having the same deficiencies as the claims they depend from.

Appropriate correction is required.

6. Claims 10 and 12 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

As to claims 10 and 12, the specification does not further provide any explanation on how "issuing cross calls that halt the operation of all CPU's in the system" is accomplished. The Examiner is unclear how this claimed feature can be accomplished without further disclosure from the Applicant.

Appropriate correction is required.

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 1-7, 9, 10, 11, 12, 13-25 and 27 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As for claims 1-7, the limitation "said testing" lacks sufficient antecedent basis. The claim previously mentions "determining", not "testing".

As for claims 7, 9, 14 and 27, the Examiner is unclear what qualifies as "necessary" as intended by the Applicant. The specification makes no further explanation regarding the degree of necessity.

As for claims 10 and 12, the limitation "operation of all CPU" lacks sufficient antecedent basis. Furthermore, the Examiner is unclear which operation of all CPU's in

the system is being referred to by the Applicant. Is it the only particular operation that the CPU's were performing when the miss exception handler was invoked, or any operation that is performed by the CPU's at any time, such as a thread or process that was put in sleep or wait mode, or simply any operation that can be performed by the CPU's, or are the CPU's are halted from doing any operations at all?

As for claims 11 and 12, the limitation "said resources" lacks sufficient antecedent basis. The Examiner is unclear if it is referring to the translation storage buffer and the page tables, or just one of them. The claims are rejected in view of the former interpretation.

As for claims 13-25, the limitation "operation of the memory management unit" lacks sufficient antecedent basis. Furthermore, the Examiner is unclear which operation of the memory management unit is being referred to by the Applicant. Is it an instruction being executed before invoking the miss exception handler, or something else?

All dependent claims are rejected as having the same deficiencies as the claims they depend from.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. Claims 13, 14 and 26 are rejected under 35 U.S.C. 102(b) as being anticipated by Mohamed et al. [5,899,994] (hereinafter "Mohamed et al.").

As for claim 13, Mohamed et al. teaches a method of handling translation lookaside buffer (TLB) miss exceptions in a memory management unit (Fig 3, combination of 52, 82 and 84) of a multi-processor computer system having a plurality of CPU's (Fig 5, CPU 1-N; Fig 12, Processor(s); Column 6, lines 30-35), the method comprising:

determining that a TLB miss exception event has occurred (TLB miss traps into the operating system kernel, see Column 2, lines 5-13);

invoking a miss exception handler (TLB software trap handling, see Column 2, lines 52-67 to Column 3, lines 1-25);

determining the nature of the TLB miss exception event (the nature of the exception, such as the address value not found in the TLB, must be determined by the TLB software trap handler, in order to resolve the exception);

resolving the miss exception event (see column 3, lines 6-25); and

returning to the operation of the memory management unit (the memory access which caused the TLB miss has the correct mapping to continue, see column 3, lines 6-25).

As for claim 14, Mohamed et al. further teaches resolving of the miss exception event includes selectively pausing the miss exception handler when necessary until the miss exception event is resolved (if hash table 84 must be searched to find the correct mapping if it is not found in TSB 82, then the handler must pause/wait for some period of time until the search is complete, see column 3, lines 15-25).

As for claim 26, Mohamed et al. teaches a method of accomplishing memory management of miss exceptions in a memory management unit (Fig 3, combination of 52, 82 and 84) of a multi-processor computer system (Fig 5, CPU 1-N; Fig 12, Processor(s); Column 6, lines 30-35), the method comprising:

determining that a miss exception event has occurred (TLB miss traps into the operating system kernel, see Column 2, lines 5-13), wherein the miss exception event concerns one of: an unassigned context identifier event, a memory access event changing a shared memory resource (a TLB miss caused by a memory write operation to 906 Primary Storage, which is a shared RAM by the CPUs, the RAM is used to store executable program code, see Fig 12 and Column 12, lines 5-10; Column 12, lines 40-56), a TSB resizing event; and

resolving the miss exception event in accordance with a miss event resolution protocol suitable for resolving the received miss exception event (TLB software trap handling, see Column 2, lines 52-67 to Column 3, lines 1-24).

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 1, 2, 3, 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Khalidi et al. [5,956,756] (hereinafter "Khalidi"), in further view of Mohamed [US 6,427,162 B1] (hereinafter "Mohamed") and Mohamed et al. [5,899,994] (hereinafter "Mohamed et al.").

As for claim 1, Khalidi teaches a memory access method for use in a memory management unit (MMU) (Fig 2, MMU) of a computer system (see Fig 1) having a plurality of interconnection central processing units (CPU's) controlled by the same operating system ("the operating system", see column 12, lines 46-50; column 1, lines 35-40) and MMU (column 1, lines 30-35; Fig 2, MMU), the method comprising:

A) initiating a memory access instruction concerning a selected virtual address (column 3, lines 66-67; column 4, line 1);

B) searching a translation lookaside buffer (TLB) for a TLB entry having the selected virtual address (column 4, lines 1-12);

C) wherein a TLB entry having the selected virtual address is found in the TLB:

accessing an associated physical address translation from the TLB entry and executing the memory access instruction (column 3, lines 66-67; column 4, lines 1-12 and 34-46);

D) where the a TLB entry having the selected virtual address is NOT found in the TLB:

i) determining whether a translation table entry (TTE) corresponding with the selected virtual address is available in secondary memory assets of the system to have memory access instructions performed thereon (secondary memory asset comprises TSB, see column 4, lines 46-59; column 6, lines 41-67; column 7, lines 1-20 and 30-47),

E) wherein the TTE is available:

i) accessing the TTE from the secondary memory assets (column 7, lines 30-47);

ii) updating at least one of the TLB and the secondary memory assets with information from the TTE (Fig 8, 860; column 12, lines 7-39); and

iii) returning to A) initiating a memory access instruction (since this translation is completed, the MMU waits for the next access instruction to be initiated if there is one); and

F) wherein said testing determines that the TTE is not available:

i) selectively pausing the method until the TTE becomes available (search in Level III takes some period of time to complete, therefore the memory must pause/wait for it to complete, as it depends on the result of the research, see column 4, lines 60-67; column 5, lines 1-5 and 18-27); and

ii) returning to A) initiating a memory access instruction (same as (E) (iii)).

Although Khalidi does not specifically disclose that the virtual address "having an associated context identifier", it does suggest it (a TLB entry is associated with a TSB entry, which has a context identifier, and therefore it is also associated with a context identifier, see column 8, lines 66-67; column 9, lines 1-13; column 12, lines 7-39; Fig 5, 530 Context Number). Furthermore, Mohamed teaches virtual memory management system wherein a virtual address in a TLB entry has an associated context identifier in order to uniquely identify a process (see column 2, lines 20-25 and Fig 1b, 178). Therefore, it would have been obvious to one ordinarily skilled in the art at the time of

the Applicant's invention to have an associated context identifier for a virtual address in order to uniquely identify a process.

Furthermore, although Khalidi does not specifically disclose that the computer system is a multi-processor computer system, it does teach a multi-processor computer system using virtual memory (column 1, lines 45-49; column 3, lines 14-19). Mohamed et al. teaches a multi-processor computer system implemented with a similar virtual memory management system as described in claim 26 using the same operating system ("the operating system", see column 3, lines 6-24) and MMU (Fig 3, combination of 52, 82 and 84), as a multi-processor computer system provides more computing capabilities and faster speed than a single processor system. Therefore, it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention to implement Khalidi's computer system as a multi-processor computer system in order to improve computer power and speed.

As for claim 2, Khalidi further teaches in D) (1) determining whether a TTE corresponding with the selected virtual address is available in secondary memory assets includes testing the associated context identifier to determine the availability of the TTE to have a memory access instruction performed thereon (see column 9, lines 7-13).

As for claim 3, Khalidi further teaches testing the associated context identifier is performed prior to accessing the TTE from the secondary memory assets (the test is be done prior to accessing to determine a hit, see column 9, lines 7-13).

As for claim 4, Khalidi further teaches updating at least one of the TLB and the secondary memory assets with information from the TTE includes updating with information including physical address information (see column 12, lines 10-13).

As for claim 5, Khalidi further teaches updating at least one of the TLB and secondary memory assets with information from the TTE includes updating with information including attribute information (translation information updated to the TLB is attribute information needed for address mapping, also the information updated to the TSB from Level III is attribute information, see column 5, lines 18-27; column 12, lines 7-39).

13. Claims 6 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Khalidi [5,956,756] and Mohamed [US 6,427,162 B1], in further view of Mohamed et al. [5,899,994] (hereinafter "Mohamed et al.") and Microsoft Computer Dictionary (hereinafter "Microsoft").

As for claim 6, the claim is already substantially discloses by Khalidi in view of Mohamed and Mohamed et al as described above, but the combined references fail to

teach "iv) invoking a miss exception handler to facilitate resolution of a miss exception event ...". However, Microsoft teaches that a page fault (also known as Virtual Memory Exception) is a miss exception event that is resulted when a virtual address is not found in physical memory (not found in Khalidi's Level II/TSB and Level III/Big Software Translation Table, the "said unavailability"), and a miss exception handler is invoked to facilitate resolution of the exception ("the operating system respond to the page fault by ...", see Page 387, Page Fault), the operating system then returns from handling the exception by finishing the execution of the memory access, then executes the next memory access instruction ("returning to initiating a memory access instruction"). Therefore, it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention to implement Microsoft's page fault interrupt handling to resolve a miss exception that resulted in the previously said unavailability.

As for claim 8, the claim is already substantially disclosed as described above by claim 6 as described above, but claim 6's references fail to specifically disclose a computer readable media including computer program code to perform the limitations presented in steps (A) to (E). Step (F) is performed by computer program code as claim 6 discloses that a page fault is detected and handled by the operating system, which then returns from handling the page fault. However, Mohamed et al. further teaches a computer readable media include computer program code (RAM, see column 12, lines 5-10 and 40-56) to perform virtual memory management operations including TSB management and virtual to physical address translation (see column 12, lines 40-47). It

is clear that computer software program is a more flexible implementation than hardware, and there it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention to implement computer program code included in a computer readable media to perform the operations described by claim 8.

14. Claims 7, 9, 22 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Khalidi [5,956,756], Mohamed [US 6,427,162 B1], Mohamed et al. [5,899,994], and Microsoft Computer Dictionary (hereinafter "Microsoft"), in further view of Data Structures, Algorithms, and Applications in Java by Sartaj Sahni (hereinafter "Sahni").

As for claim 7, 22 and 23, the claims are already substantially disclosed as described above, but the combined references in claim 6 fail to teach "determining the nature of the miss exception event; selectively pausing ... has been resolved;". However, Sahni teaches that in handling an exception event, the nature of the miss exception is determined in order to properly resolve an exception based on its type (see page 15, Handling Exceptions, and page 16, catch block and exception type in program 1.6). The program code inside the catch block code requires a certain amount of time to execute, and even possibly invoke another method outside the miss exception handler ("selectively pausing the operating ... ", see page 16, program 1.6, calling System.out.println(e) inside catch (Throwable e)). Therefore, it would have been

obvious to one ordinarily skilled in the art at the time of the Applicant's invention to combine Sahni's teaching with those of the combined references in claim 6 in order to properly resolve the exception event.

It is also clear that claims 22 and 23 are already substantially disclosed by claim 7, except for claim 23, the secondary memory assets include both the Level II TSB and the Level III Big Software Translation Table (page table) described in claim 1, and step (B) (2) of claim 22 is performed by the page fault handling method described in claim 7.

As for claim 9, it is clear the claim is already substantially disclosed as described above by claim 7, while applying the same motivation for combining Khalidi, Mohamed, Mohamed et al., and Microsoft as described in claim 8.

15. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Khalidi [5,956,756], Mohamed [US 6,427,162 B1], Mohamed et al. [5,899,994] and Microsoft, in further view of Wu et al. [5,906,001] (hereinafter "Wu").

As for claim 10, Khalidi in further view of Mohamed already substantially discloses the claims as described above, but fails to teach that the computer program code instructions include computer program code instructions for invoking a miss exception handler without issuing cross calls that halt the operation of all CPU's in the system. However, Wu teaches computer program code instructions (see column 4, lines 58-67) for handling TLB miss (TLB shootdown operation, see column 3, lines 12-

15) in a multiprocessor system (see Abstract and Fig 3) that does not issue cross calls (inter-processor interrupts are cross calls, see column 2, lines 50-63) that halt the operation (see Abstract and column 3, lines 18-20), in order to avoid invoking interrupt handler routines and reduce the amount of time required to invalidate multiple TLBs (see column 2, lines 64-76 and column 3, lines 12-20). Therefore, it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention to combine Wu's teaching with that of Khalidi and Mohamed et al.'s combined teaching in order to avoid invoking interrupt handler routines and reduce time consumption in TLB invalidation.

16. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Khalidi [5,956,756], in further view of Mohamed [US 6,427,162 B1], Mohamed et al. [5,899,994], Microsoft and Sahni, in further view of Computer Architecture by Patterson and Hennessy (hereinafter "Patterson") and Operating Systems by Tanenbaum and Woodhull (hereinafter "Tanenbaum").

The claim is already substantially disclosed as described above in claims 1, 6, 7, 22 and 23, but the previously cited references fail to teach "each CPU having a memory cache configured to include a translation lookaside buffer (TLB)" and "secondary memory assets that include page tables" (claim 23 only mentioned "at least one page table"), although Mohamed et al. does teach a multi-processor system wherein a TLB is included in each CPU (see Mohamed et al., Fig 2).

However, Patterson teaches a multi-processor system wherein each CPU has a memory cache (see page 638, Fig 8.1) in order to reduce latency and avoid incoherency as compared to having shared cache(s) for all CPU's. Therefore, it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention to have, for each CPU in a multi-processor system, a memory cache configured to include a TLB, in order to reduce access latency and avoid incoherency, and the memory cache is an conveniently available fast storage for storing the TLB, in order to enable fast access by the CPU.

Furthermore, although Khalidi already discloses that the secondary memory assets include a TSB and a page table, it failed to teach page tables included in the said assets. However, Tanenbaum teaches a virtual memory management technique wherein multiple pages arranged in a hierarchy are used to reduce page table lookup time and to avoid keeping huge page tables in memory all the time (see page 324, second paragraph and Multilevel Page Tables, also page 325, Fig 4-10). Therefore, it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention to combine Tanenbaum's teaching with the references previous cited in order to reduce page table lookup time and to avoid keeping huge pages tables in memory all the time.

17. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Khalidi [5,956,756], Mohamed [US 6,427,162 B1], Mohamed et al. [5,899,994], "Patterson" and "Tanenbaum", Microsoft and Sahni, in further view of Wu [5,906,001].

As for claim 12, it is clear the claim is already substantially disclosed by claims 10 and 11 as described above.

18. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mohamed et al. [5,899,994], in further view of Mohamed [US 6,427,162 B1].

As for claim 15, Mohamed et al. already substantially discloses the claim as described above, but fails to teach that "determining that a TLB miss exception ..... whether a TLB miss exception has occurred". However, Mohamed teaches a similar method of handling TLB miss wherein determining a TLB miss exception event has occurred includes testing a context identifier for the affected virtual address to determine whether a TLB miss exception has occurred (see column 7, lines 10-16 and lines 30-35), in order to detect a TLB miss and generate a trap to handle it (see column 7, lines 30-32), and the context identifier is included in a TLB entry to be associated with a virtual address in order to uniquely identify a process associated with the virtual address (see column 2, lines 20-25). Therefore, it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention to combine Mohamed's teaching with that of Mohamed et al's in order to uniquely identify a process and detect a TLB miss.

Allowable Subject Matter

19. Claims 28 and 29 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

20. The following is an examiner's statement of reasons for allowance:

As for claim 28, Mohamed teaches resizing a translation storage buffer/TSB (see column 5, lines 3-12; column 10, lines 25-34), but fails to teach that the resize concerns an exception, which is resolved by "activating a lock for the TSB to prevent other processes from accessing entries ..... releasing the lock on the TSB".

As for claim 29, Mohamed teaches invalidating TSB contexts (see column 4, lines 34-45), but fails to teach an unassigned context identifier which concerns an exception event, which is resolved by "assigning a context identifier for a virtual address space associated with a TSB; and assigning a portion of memory to the TSB".

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shawn Gu whose telephone number is (571) 272-0703. The examiner can normally be reached on 9am-5pm, Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald Bragdon can be reached on (571) 272-4204. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shawn X Gu
Patent Examiner
Art Unit 2189

REGINALD G. BRAGDON
PRIMARY EXAMINER

28 March 2006